Ohio Scientific Micro Devices
**OSI PULSE GENERATOR, PULSE DETECTOR**

There are 8 pulse outputs. Each output is associated with one bit of the 8-bit data word at micro address 32,785 (8011 Hex.).

<table>
<thead>
<tr>
<th>PULSE #</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA BIT #</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>BIT VALUE</td>
<td>128</td>
<td>64</td>
<td>32</td>
<td>16</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

To generate a pulse the associated bit at location 32785 must be turned on (1) with a memory write operation. For example, to generate Pulses #5 and #3 simultaneously, write a 40 (32+8 in decimal, 0010 1000 in binary, 28 in hexadecimal) into address 32785 (8011 hex). A 12 volt, 0.6 millisecond pulse will then result at Pulse Outs #5 and #3.

<table>
<thead>
<tr>
<th>PULSE IN#</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA BIT#</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>BIT VALUE</td>
<td>128</td>
<td>64</td>
<td>32</td>
<td>16</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

A pulse occurring at one of the pulse inputs will automatically turn on the associated bit at location 32784. The memory location can be read to see which inputs received pulses since the last read operation. After each read operation the 8-data bits are automatically cleared to zero again.

For example, suppose a pulse occurs at pulse inputs #6 and #3. If memory location 32784 is then read, the number 72 (64+8 in decimal, 0100 1000 in binary, 48 in hexadecimal) will be found there. If location 32784 is immediately read again the number 0 will be found, showing that the read operation did result in clearing the word.
The pulse detector also has interrupt capabilities. Whenever one or more of address 32784's data bits are on (1), then the microcomputer's IRQ interrupt request line is pulled low, the IRQ line returns high when the pulse detector address is cleared again by a read operation.

Any number of devices can pull the IRQ line low, the Hybrid being one of them. Address location 32771 (8003Hex) is set up to enable the user to determine which device is requesting an interrupt, The Most Significant Bit is assigned to the Hybrid Synthesizer, and the Least Significant Bit is assigned to the Pulse Detector. If the bit is on (1), then that device is the interrupting device. Note that this is also a means of detecting a pulse occurrence without clearing the pulse detector address location.

The IRQ interrupt request line is normally masked by the 'I' bit of the 6502 processor status register being set to 1. Entering BASIC automatically sets this bit. It can also be set by the SEI machine code instruction or by loading 04Hex into location O12C_Hex (the Monitor Program's Go and Break-point location for the Status Register).

When the IRQ Mask Bit I in the 6502 Status Register is cleared to 0, the interrupt routine is enabled. When the IRQ line goes low the Microcomputer stops whatever it is doing in order to service the interrupt. It will go to the address 01C0Hex (448Dec) expecting to find there a user loaded subroutine to deal with the interrupt.
OSI DIGITAL TO ANALOG CONVERTERS (DAC)

There are 8 DACs found at micro address locations 32800 through 32807 (8020 to 8027 Hex). The 8-bit data word written into one of these address locations is converted to a voltage level appearing at one of the front panel's 8 DAC output jacks.

Note that the DACs use only the Write function of the address locations. Reading into the same locations will access the ADCs, not the DACs.

An 8-bit data word provides for 256 possible voltage levels at the DAC output. As the data word is incremented from zero to 255 the output voltage goes from zero volts to some maximum. The maximum voltage is set by a DAC volume control which affects all 8 DACs simultaneously. Thus the maximum voltage can be varied from about 2 volts to 12 volts. The step size also changes by the value $V_{max}/255$.

The 8 DACs are actually multiplexed. That is, one converter is used to convert the 8 digital input words one at a time. The result is held in a sample-and-hold circuit until the converter comes back around to that one input word again. This, of course, is done at a high speed - one conversion takes 4 microseconds. The sampling rate for each output is 31.25 KHz. Thus the DACs can handle audio signals as high as about 15 KHz.
OSI ANALOG TO DIGITAL CONVERTERS (ADC)

There are 8 ADCs found at micro address locations 32800 through 32807 (8020 to 8027 Hex). The 8-bit data word read from one of these address locations is derived from the voltage appearing at one of the front panel's 8 ADC input jacks.

Note that the ADCs use only the Read function of the address locations. Writing into the same locations will access the DACs, not the ADCs.

The ADCs accept voltage input levels from zero to 5 volts. A zero volt input is converted into a zero value 8-bit word. Any voltages lower than zero volts are also converted to the zero value. A 5 volt input level is converted to the number 255. Any voltages above 5 volts are also converted as 255.

The input to each ADC has been designed with an AC/DC switch in order to accommodate both signal and control voltage inputs. Also, an attenuator control has been placed on each input so that one can adjust for the 0 to 5 volt input limitations. The input circuitry works as follows:

1) with no signal input and the input switch on 'CV'
   The Attenuator control acts as a variable voltage from 0 to 5 volts,

2) with a Control Voltage input and the input switch on 'CV' the actual signal going to the ADC is an attenuated Control Voltage. The Control pot should be adjusted so that 255 is read with the maximum CV input.

3) With a Signal input and the input switch on 'SIG' the actual signal going to the ABC is an attenuated signal offset to 2.5 volts. The output values read, then, vary around the bias value 127.
The 8 ADCs are actually multiplexed. That is, one converter is used to convert all 8 inputs one at a time in succession. Since the ADC used is relatively slow this multiplexing scheme severely limits the frequency range the ADC can handle. A compromised solution to this problem has been worked out. It centers around the 3-position switch marked '8 4 2'. In the '8' position, all 8 inputs are converted at the slowest sampling speed and thus the most severe frequency input limit. In the '4' position, only ADC inputs 0, 1, 2, 3 are converted at twice the sampling rate. Finally, in the '2' position, only ADC inputs 0 and 1 are converted at 4 times the sampling rate.

The chart below shows the resulting high frequency limitations for each of the 3 switch settings. It is based on a single conversion time of 125 microseconds,

<table>
<thead>
<tr>
<th>SWITCH POSITION</th>
<th>INPUTS CONVERTED</th>
<th>SAMPLING FREQUENCY</th>
<th>MAXIMUM INPUT FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0,1</td>
<td>4KHz</td>
<td>2KHz</td>
</tr>
<tr>
<td>4</td>
<td>0, 1, 2, 3</td>
<td>2 KHz</td>
<td>1KHz</td>
</tr>
<tr>
<td>8</td>
<td>All 8</td>
<td>1KHz</td>
<td>500 Hz</td>
</tr>
</tbody>
</table>
The AY-3-8912 PSG is a Large Scale Integrated Circuit Chip which can produce a variety of complex sounds under software control. The chip has three 1-volt peak-to-peak square wave signal outputs. The user can control the pitch, amplitude, tone/noise mix, and envelope of these outputs.

The chip contains 16 data registers which the user loads to control the various sound parameters. These 16 registers are entered via two micro address ports.

First, the number of the register to be loaded (0 - 15) must be written into micro address 32787 (8013 Hex). (Take care, the register numbers in the Manual are in octal form.)

Second, the data to be loaded into the register must be written into micro address 32786 (8012 Hex). This step can be repeated any number of times until you want to change the register in which case you return to step one.
Pulse Generator

AY-Synthesizer

801216 Load Data
801316 Load Register #